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DICKE, BILLIG & CZAJA
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET, SUITE 2250
MINNEAPOLIS, MN 55402

EXAMINER	
WOLVERTON, DAREN A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,483	HAGEN ET AL.	
	Examiner	Art Unit	
	DAREN WOLVERTON	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/31/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 16-18 24, 26-28, and 31-33 are objected to because of the following informalities: these claims uses the term "comprising wherein", "comprising where", and "comprising" when they should use either "further comprising" (for reciting additional components) or "wherein" (for reciting additional limitations involving already recited components). Appropriate correction is required.

Claim 26 is objected to because of the following informalities: the term "the wiring substrate" lacks antecedent basis, though clearly it was meant to be "the wiring carrier". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15-24, 18, 25-28 and 30-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 15 and 30, these claims recite the limitation "contact areas of an integrated circuit of the active upper side of the semiconductor chip and/or the external contact together with the contact pads are electrical connect to one another via wiring lines and/or through contacts of the wiring substrate" and it is unclear as to what exactly is connected to what. As best as can be determined by the examiner, it is meant

that either the contacts of the chip are connected to the contact pads on the substrate via wiring lines or the external contacts on the bottom of the wiring substrate are connected to those on the top of the wiring substrate using through holes or wiring lines. Likewise, all claims dependent on claims 15 and 30 are also rendered indefinite.

Regarding claims 18 and 30, these claims recite a base semiconductor chip and it is unclear if this is a separate chip than the earlier recited semiconductor chip, however it appears from the specification that they are the same chip and will be treated as such for the purpose of this action. Additionally, these claims recite the term "concomitantly" which means "at the same time as" or "accompanying in a subordinate way" and it is unclear how that affects the arrangement of the interconnecting film. In order to enable prosecution the claims will be treated as if the word "concomitantly" was omitted. Likewise, all claims dependent on claims 18 and 30 are also rendered indefinite.

Regarding claim 25, the term "the intermediate carrier film" lacks antecedent basis rendering the claim indefinite, as best as can be determined by the examiner "the deformable interconnection film" is meant. Likewise, all claims dependent on claim 25 are also rendered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15-17, 20-21, 23, 29 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Goller et al. (US 2003/0042591, henceforth Goller).

Regarding claim 15, Goller, in FIG. 3, disclose a base semiconductor component (consisting of everything below the part labeled 10 in the figure) comprising a stiff wiring substrate 8 (called a flat carrier substrate by Goller, note that paragraph [0032] discloses that it is composed of ceramic or epoxy materials used for PCBs, implying that it is stiff) having contact pads 82 (called contact surfaces by Goller) on its upper side 81 in edge regions (see FIG. 3) and external contacts 14 (called additional contact bumps by Goller) of the base semiconductor component on its underside 83; a semiconductor chip 4 arranged on the upper side 81 of the stiff wiring substrate 8 opposite the external contacts 14 (see FIG. 3) , the semiconductor chip 4 having an integrated circuit on an active upper side (paragraph [0028]) with contact areas 43 (paragraph [0028] and FIG. 1); a deformable (paragraph [0021]) interconnection film 10 (called an intermediate carrier by Goller) having conductor tracks (paragraph [0031]), wherein the deformable interconnect film 10 defines the upper side of the base component and is deformed (note as this is a product claim, deformed is read as bending towards not formed by deformation) in its edge regions toward the contact pads of the wiring substrate (see FIG. 3); wiring lines or through contacts of the wiring substrate that electrical connect the contact pads 82 to the to the external contacts 14 (see the 112 rejection above) (paragraph [0016]); and stack contact areas 104 (called

second terminal contacts) arranged in a freely accessible arrangement pattern and congruently with respect to external contacts of a semiconductor component to be stacked (second semiconductor chip 6, in FIG. 3), wherein the stack contact areas are electrically connected to the contact pads 82 of the stiff wiring substrate 8 via the conductor tracks of the interconnection film 10 (paragraph [0031]).

Regarding claim 16, Goller further discloses that the semiconductor chip has flip-chip contacts (paragraph [0019]) which are connected via wiring lines (the conductive traces in the interconnection film 10, note that the claim does not specify the location of the wiring lines) to the contact pads 82 and via wiring lines on the upper side and through contacts to the underside of the wiring substrate, and also via wiring lines on the underside of the wiring substrate 8 to external contact areas, to the external contact areas having the external contacts 14 (implied by paragraph [0016] which discloses that the carrier substrate is a rewiring board).

Regarding claim 17, Goller further discloses that the external contacts 14 have solder balls (implied by FIG. 3 and by paragraph [0032] which describes them as additional contact bumps and paragraph [0032] which describes the previous contact bumps as solder balls) and are arranged on the underside 83 of the wiring substrate 8 in a matrix (shown in FIG.3, a matrix being read broadly as a pattern)

Regarding claim 20, Goller, in paragraph [0030], further discloses that the base semiconductor component and the stacked semiconductor component 6 are electrically connected via the stack contact areas 104 of the interconnection film 10.

Regarding claim 21, Goller, in paragraph [0031], further discloses that the interconnection film 10 has a plurality of mutually insulated layers (two in this case, one on top and the other on the bottom) with conductor tracks.

Regarding claim 23, Goller, in FIG. 3 and paragraph [0039], further discloses that the semiconductor chip 4 of the base substrate component is electrically connected to the contact pads via bonding wire connections 106. Note that in this rejection all of the contact pads of the stiff wiring substrate 8 are considered part of the same group.

Regarding claim 29, Note that Goller, in FIG. 3, discloses that the semiconductor chip is arranged centrally and that all other limitations of this claim are disclosed in the claim 15 rejection above.

Regarding claim 34, Note that Goller, in paragraph [0034] through paragraph [0040], discloses a means for providing a semiconductor chip 4 arranged centrally on a stiff wiring substrate 8 (called a flat carrier substrate) (paragraph [0034]) and a means for providing contact pads 82 (called contact surfaces) in edge regions of the wiring substrate 8, which are electrically connected to external contacts 14 (called additional contact bumps) and at the same time to contact areas 43 (first solder contact surfaces) of the semiconductor chip 8 and also to stack contact areas 104 (second terminal pads); and the stack contact areas 104 form an upper side of the base semiconductor component (see FIG. 3) and have an arrangement pattern corresponding to an arrangement pattern of external contacts of a semiconductor component 6 to be stacked (paragraph [0034] through paragraph [0040]).

Claims 15, 19, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Chun (US 6,291,259).

Regarding claim 15, Chun FIG. 3 discloses a base semiconductor component for a semiconductor component stack (see FIG. 4) comprising: a stiff wiring substrate 21 (called a supporting member by Chun) having contact pads (column 3, lines 8-13, with contact pads being broadly read as surfaces which make contact between to conductors) on its upper side in edge regions (see FIG. 3) and external contacts 24b (called connecting portions by Chun) of the base semiconductor component on its underside (see FIG. 3); a semiconductor chip 1 arranged on the upper side of the stiff wiring substrate 21 opposite the external contacts (see FIG. 3), the semiconductor chip 1 having an integrated circuit on an active upper side (not explicitly stated but implied as one of ordinary skill in the art would recognize that most semiconductor chips have this) with contact areas 6; wiring lines 24a (called metal traces by Chun) or through contacts 26 (called metal patterns by Chun) of the wiring substrate that electrical connect the contact pads to the to the external contacts (column 3, lines 8-13)(see the 112 rejection above); a deformable interconnection film 4 (called metal traces by Chun, note that film is being read broadly as a thin layer) having conductor tracks (the metal traces themselves), wherein the deformable interconnect film 4 defines the upper side of the base component (see FIG. 3) and is deformed (note that as this is a product claim deformed is read as bent towards rather than created by deformation) in its edge regions 4c (see FIG. 3) toward the contact pads of the wiring substrate 21; and stack contact areas 8a arranged in a freely accessible arrangement pattern (see FIG. 3) and

congruently with respect to external contacts of a semiconductor component to be stacked (see FIG. 4), wherein the stack contact areas 8a are electrically connected to the contact pads of the wiring substrate via the conductor tracks of the interconnection film 4 (see FIG. 3).

Regarding claim 19, Chun further discloses a supporting plate 2 (called an elastomer by Chun) arranged between the interconnection film 4 and the semiconductor chip 1.

Regarding claim 22, Chun further discloses, in FIG.3 and FIG. 5E-FIG.5F, that the semiconductor chip 1 of the base semiconductor component is embedded in a plastics composition 28 (called an encapsulate or molding resin by Chun).

Regarding claim 24, Chun further discloses in FIG. 3, that the connection locations (at the point labeled 4c in FIG. 3) between contact pads and conductor tracks of the interconnection film 4, in the edge regions of the wiring substrate 21, are embedded in a plastic covering 28 (called an encapsulate or molding resin by Chun).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goller in view of Roeters et al. (US PGPUB 2003/0111736. henceforth Roeters).

Regarding claim 18, Goller, as described in the 102 rejection section, discloses all of the limitations of claim 15 but does not disclose that the interconnection film is arranged on the rear side of the semiconductor chip (see the 112 rejection section above).

Roeters, in FIG. 3, discloses a similar base stack device, in which the interconnection film 112 (called a flex circuit by Roeters) is arranged on the rear side of the semiconductor chip 128 (called an integrated circuit chip package).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Goller by inverting the semiconductor chip 4 (such that the conductive contacts face down and the interconnecting film 10 is arranged on the rear side of the semiconductor chip). One of ordinary skill in the art at the time of the invention would be motivated to do this in order to create an even surface for the placement of the interconnection film or to simplify the wiring pattern on the lower side of the interconnection film.

Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goller and Roeters as applied to claim 18 above, and further in view of Chun.

Regarding claim 30, the modified invention of Goller and Roeters discloses all of the limitations of claim 30 (as described in the rejections to claim 1 in the 102 section

and claim 18 above) except that a supporting plate is arranged between the interconnection film 10 and the semiconductor chip 4.

Chun, FIG. 3, discloses a base semiconductor component for a semiconductor component stack, in which a supporting plate 2 (called an elastomer by Chun) is arranged between the interconnection film 4 (called metal traces by Chun, note that film is being read broadly as a thin layer) and the semiconductor chip 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the combined invention of Goller and Roeters by adding a supporting plate between the rear side of the semiconductor chip 4, and the interconnection film 10. One of ordinary skill in the art at the time of the invention would be motivated to do this in order to avoid unwanted distortion of the flexible substrate during processing.

Regarding claim 31, Goller further discloses in FIG. 3 and paragraph [0030], electrically connecting the base semiconductor component and the stacked semiconductor component 6 via the stack contact areas 104 of the interconnection film 10.

Regarding claim 32, Goller, in paragraph [0031], further discloses that the interconnection film 10 has a plurality of mutually insulated layers (two in this case, one on top and the other on the bottom) with conductor tracks.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goller, Roeters, and Chun as applied to claim 18 above, and further in view of Lee (US PGPUB 2003/0134450).

Regarding claim 33, the combined invention of Goller, Roeters, and Chun discloses all of the limitations of claim 32 but does not disclose that the semiconductor chip 4 of the base semiconductor component is embedded in a plastics composition.

Lee, paragraph [0041], discloses a method of die stacking that uses a plastic underfill material (specifically a thermoset or thermoplastic polymer) to mechanically secure flip chips to substrates.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the combined invention of Goller, Roeters, and Chun by embedding the semiconductor chip 4 into a plastic underflow material. One of ordinary skill in the art at the time of the invention would be motivated to do this in order to mechanically attach the flip chip to the substrate.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goller in view of Chun.

Regarding claim 25, Goller discloses a method for the production of a base semiconductor component comprising: producing a stiff wiring carrier 8 (called a flat carrier substrate by Goller, note that paragraph [0032] discloses that it is composed of ceramic or epoxy materials used for PCBs, implying that it is stiff) with a central semiconductor chip 4 on its upper side 81 (see FIG. 3) and contact pads 82 (called

contact surfaces by Goller) in edge regions of the upper side 81 (see FIG. 3), and also external contact areas 14 (called additional contact bumps by Goller) on its underside 83, the external contact areas 14 and the contact pads 82 and also contact areas 12 of an integrated circuit of the semiconductor chip 4 being electrically connected to one another (paragraph [0016]); producing a deformable interconnection film 10 (called an intermediate carrier by Goller) with stack contact areas 104 (called second terminal contacts) on its upper side, which have an arrangement pattern that is congruent with respect to an arrangement pattern of external contacts of a semiconductor component to be stacked (second semiconductor chip 6, in FIG. 3), and with conductor tracks on its underside (paragraph [0031]), which are connected to the stack contact areas 104 and extend right into the edge regions of the interconnection film 10 (to connect to contact pads 82), the conductor tracks having an arrangement pattern that is congruent with respect to the arrangement pattern of the contact pads (necessary to connect to them); applying the interconnection film 10 by its underside onto the wiring carrier with semiconductor chip 4 (paragraph [0035], note that the first side is the underside).

Goller differs from the claimed invention in the Goller does not disclose deforming the side edges of the interconnection film 10.

Chun, in FIG. 5C though FIG. 5E, discloses a method for the production of a base semiconductor component that brings the edges of a flexible layer 4 into contact with metal traces 26 through deformation of the flexible layer 4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Goller by bringing the side edges of the

interconnection film 10 into contact with the contact pads 82 by deforming the interconnection film 10 after placing it on semiconductor chip 10. One of ordinary skill in the art at the time of the invention would be motivated to due this in order to ensure that the interconnection film always makes good connections with the various contact pads and to avoid the complicated step of creating a U shaped interconnection film with enough rigidly to be properly placed.

Claims 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goller and Chun as applied to claim 25 above, and further in view of Caletka et al. (US PGPUB 2002/0180061, henceforth Caletka) and Chun.

Regarding claim 26, the combined invention of Goller, Chun, Roeters and Lee discloses all of the limitations of claim 25 but does not disclose that before the interconnection film 10 is applied onto the wiring carrier 8, a supporting plate is applied to the underside of the interconnection film 10.

Caletka, FIG. 5, discloses creating a flexible chip carrier 21, with a stiffener 49 that is attached to the carrier before chips are attached (paragraph [0034]).

Therefore, in view of Caletka, it would have been obvious to one of ordinary skill in the art at the time of the invention to use further modify the combined invention of Goller and Chun by attach a supporting plate (a stiffener) to the interconnection film 10. One of ordinary skill in the art at the time of the invention would be motivated to do this in order to provide a rigid contact surface for the two chips and prevent damage to the contacts due to bending.

Regarding claim 28, the combined invention of Goller, Chun, and Caletka discloses all of the limitations of claim 26 but does not disclose that the connection locations are embedded in a plastic covering after the conductor tracks (on the interconnection film 10) are connected to contact pads 82.

Chun, in FIG. 5E and FIG. 5F, further discloses embedding the completed connections in a plastic covering 28 (specifically a mold resin).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to embed the connection locations where the conductor tracks (on the interconnection film 10) are connected to contact pads 82 in a plastic covering. One of ordinary skill in the art at the time of the invention would be motivated to do this in order to protect the connection locations.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goller and Chun as applied to claim 18 above, and further in view of Roeters and Lee.

Regarding claim 27, the combined invention of Goller and Chun discloses all of the limitations of claim 25 but does not disclose that before the interconnection film 10 is applied, embedding the semiconductor chip 4 in a plastic composition.

Roeters, in FIG. 3, discloses a similar base stack device, in which the interconnection film 112 (called a flex circuit by Roeters) is arranged on the rear side of the semiconductor chip 128 (called an integrated circuit chip package).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Goller by inverting the semiconductor

chip 4 (such that the conductive contacts face down and the interconnecting film 10 is arranged on the rear side of the semiconductor chip). One of ordinary skill in the art at the time of the invention would be motivated to do this in order to create an even surface for the placement of the interconnection film or to simplify the wiring pattern on the lower side of the interconnection film.

Lee, paragraph [0041], discloses a method of die stacking that uses a plastic underfill material (specifically a thermoset or thermoplastic polymer) to mechanically secure flip chips to substrates.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the combined invention of Goller, Roeters, and Chun by embedding the inverted semiconductor chip 4 into a plastic underflow material. One of ordinary skill in the art at the time of the invention would be motivated to do this in order to mechanically secure the flip chip to the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAREN WOLVERTON whose telephone number is (571) 270-5784. The examiner can normally be reached on Monday to Thursday from 9:30 a.m. to 3:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2813

/Matthew C. Landau/
Supervisory Patent Examiner, Art Unit 2813

DW